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## **“STILL LATCHED-UP AFTER ALL THESE YEARS - MORE CLUES IN THE 7-SERIES FPGA MICRO-LATCHUP MYSTERY”**

Acknowledgments:

This work leverages test data, cooperation, and test apparatus from the XRTC (Xilinx Radiation Test Consortium).

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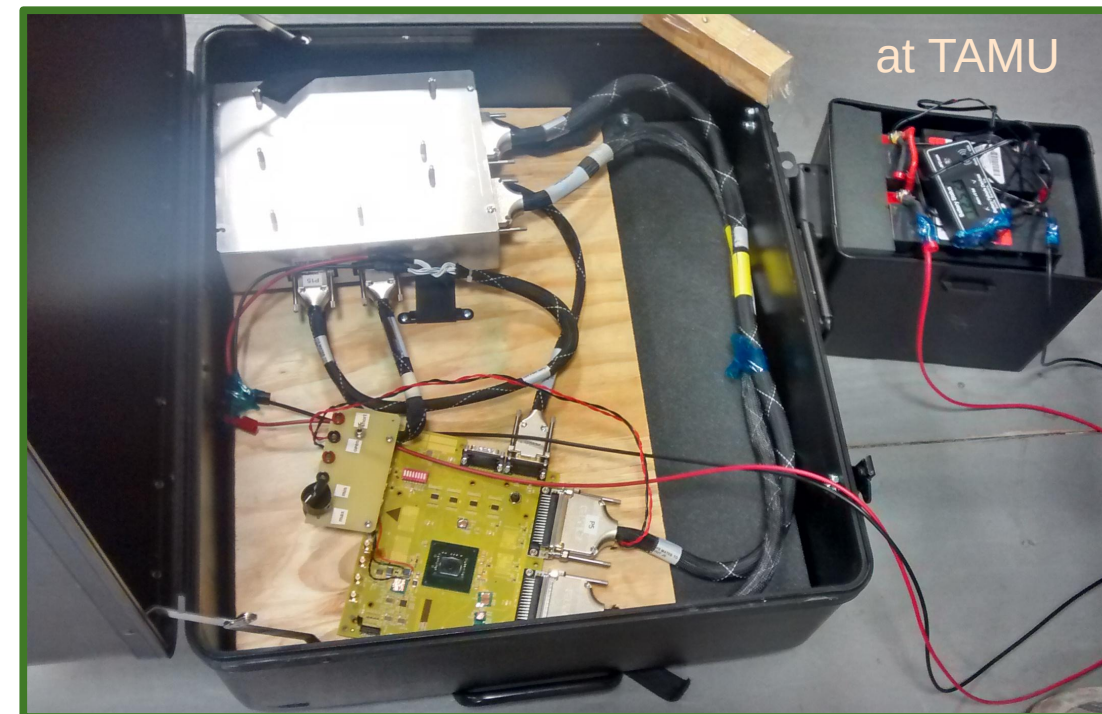
Presented at:  
SEE Symposium, Oct. 7, 2020

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# Outline



1. Motivation - Understand Space Applications' Risk from Vccaux uSEL of Xilinx 7-Series FPGAs
2. Background - What we know and how we know it
3. Main Objectives - Identify affected functionality & long-term effects, if any
4. Hypotheses "Haystack" -
  - Initial Functional Testing
  - Speed Testing
  - SERDES Testing
  - Logic Level Testing
  - AC Waveform Testing
  - Tri-State Testing
  - Level Shifting Testing
5. Future Work

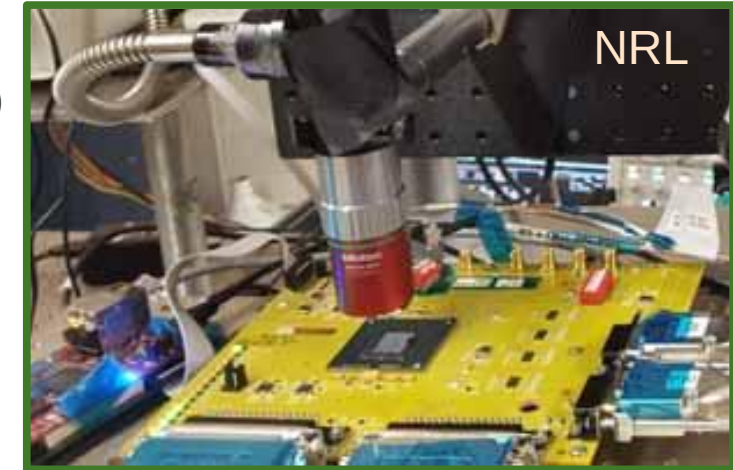




# Backstory: Find the Needle in the Haystack #1



- The Beginning:
- Discovery – XRTC's first test of 7-Series FPGAs in Sept 2013 at TAMU led by Sandia\*
  - Current steps in 1.8V Vaux rail identified as 'classical' latchup from IV characteristic: a clear holding voltage
  - Differs from 'classical' SEL in key respects:
    - SEL current steps are only about 100 mA (hence 'micro-Latchup' or 'μSEL')
    - No gross functionality problems
- The Middle:
- Haystack#1 Conquered – Harris-led investigation to locate μSEL sites\*\*
  - Custom Hardware - DUT Board (XRTC Gen2/3 compatible) and Power Board builds
  - Laser Test Campaign at NRL in May 2015
    - Three long test days and no joy: null result #1
    - 2020 hindsight: we underestimated "haystack" size significantly
      - net area coverage < 0.1%, maybe 0.01%
  - Heavy Ions Testing with Masking at TAMU in July 2015
    - Success! Localized sites to approx. two sq.mm near one corner- nowhere else
    - Maintained latchup in eight sites on six DUTs with batteries for further study

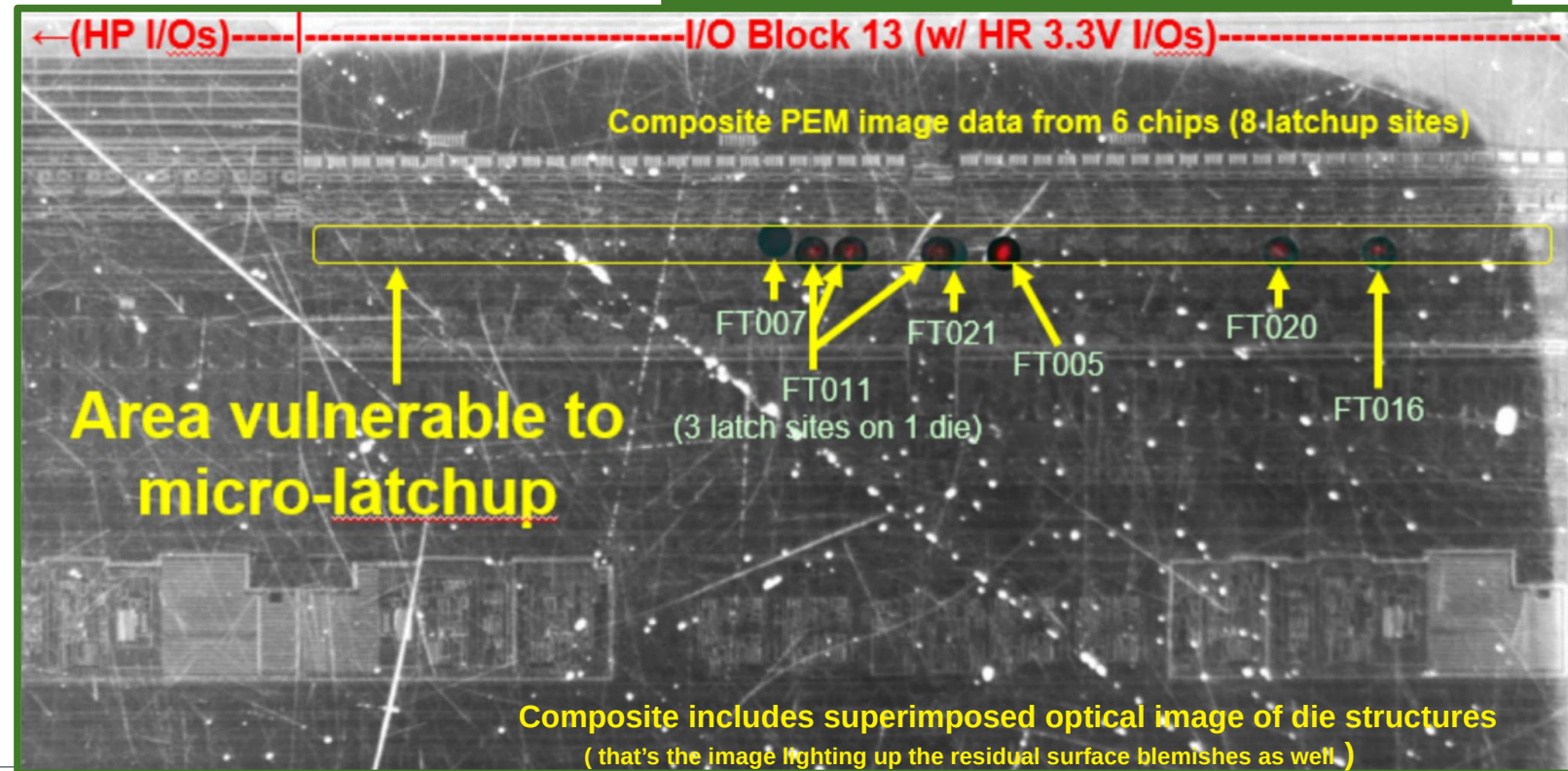
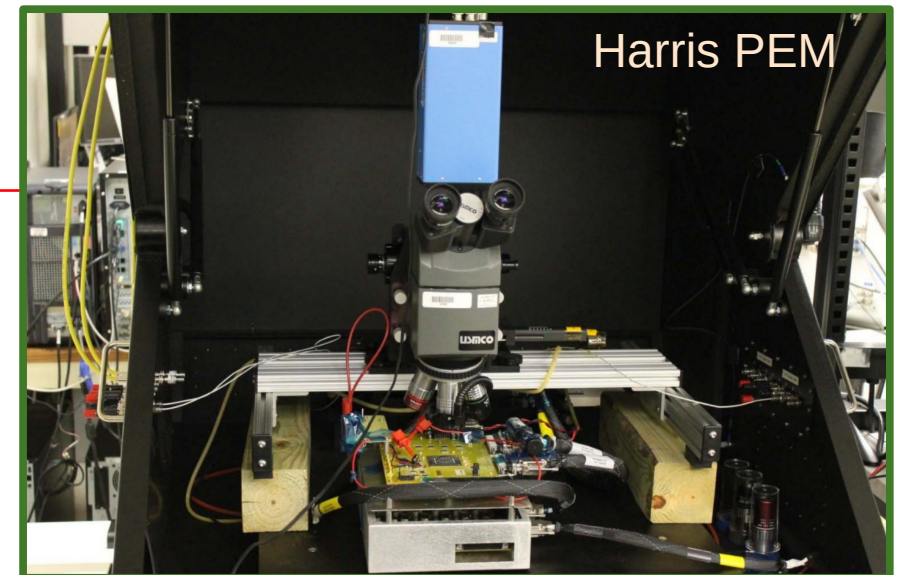


\* D.S. Lee, et al., "Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation," *IEEE Radiation Effects Data Workshop Record*, pp. 10-14, July 2014.

\*\* W. Rudge, et al., "SEL Site Localization Using Masking and PEM Imaging Techniques: A Case Study on Xilinx 28nm 7-Series FPGAs," *IEEE Radiation Effects Data Workshop Record*, July 2016.

# Backstory, cont'd

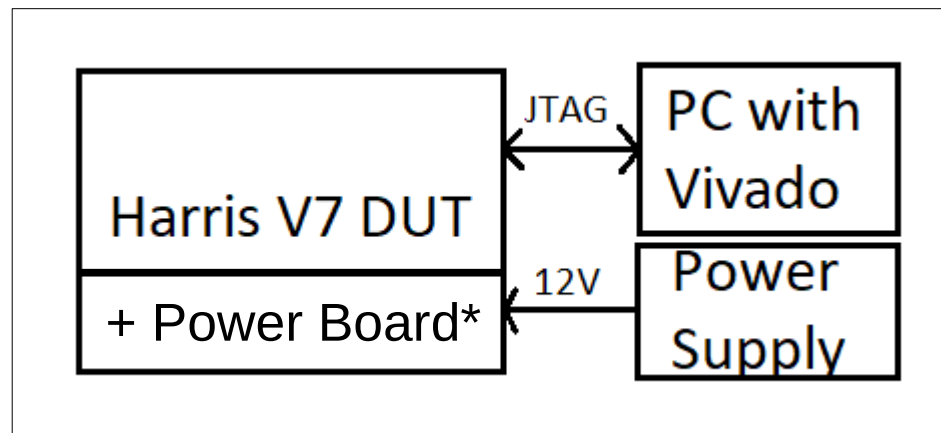
- HURRAY!
- The “Smoking Gun” found in the Harris FA lab in Florida.
- Photon Emission Microscopy (PEM) imaging reveals sites are:
  - Only in HR “high range” I/O’s
    - HR level shifter max: 3.3V
  - NOT in HP “high performance” I/O’s
    - HP max: 1.8V
- IMPORTANT NOTE:
  - Steps in 1.8V Vaux, not I/O 3.3V rail
- Backstory (2015) CONCLUSION:
  - It should be easy to find HR I/O functional problem(s) induced by the  $\mu$ SEL sites → suspect level shifter
    - Proof postponed
    - Not so easy, as it turns out



# Almost 5 Years Later - HR I/O Functionality Testing



- Initial Measurements



- Two unirradiated (control) DUTs  $V_{ccaux}$  rail currents:
  - Nominal: between 75 & 100mA
  - Expected 75mA per Xilinx\*\*
- Three DUTs still exhibit  $\mu$ SEL currents (as of Feb. 2020):
  - FT016 – 172mA
  - FT021 – 188mA
  - FT007 - 200mA
- Two (formerly) latched-up DUTs also exhibited nominal current draws on  $V_{ccaux}$  when re-powered, as expected

\* Capabilities include allowing direct measurement of the current on the separate  $V_{ccaux}$  rail.

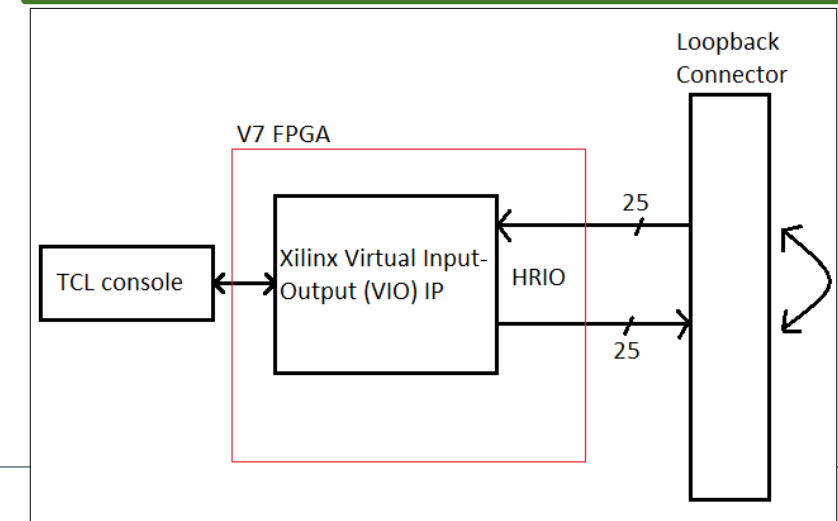
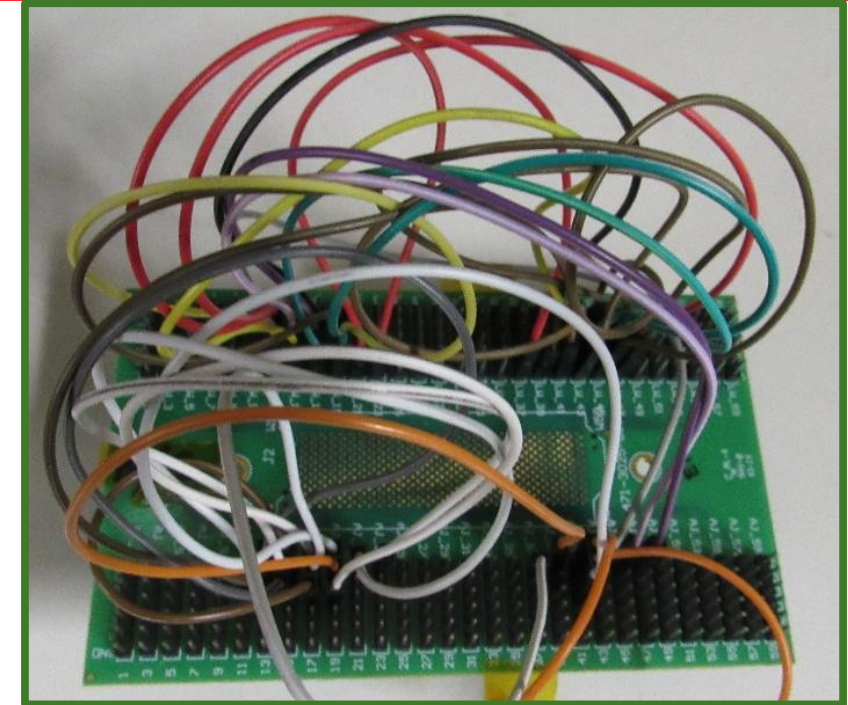
\*\* Xilinx Datasheet DS183, Page 6



# HR I/O Functionality Testing – Haystack #2 First Look



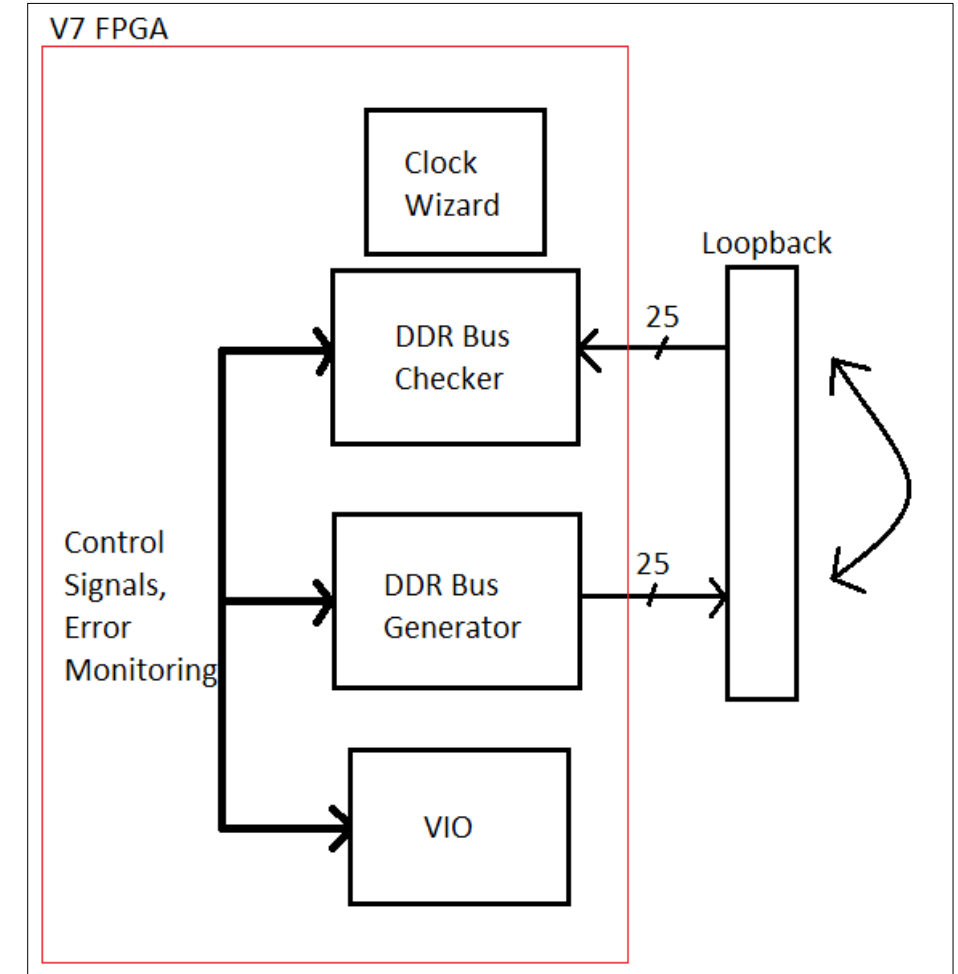
- Hypothesis #1: Level shifter malfunction
- REFINEMENT of Hypothesis #1
- Affected pin would work as input, but stuck as output
  - from Austin Lesea, Xilinx R&D Sr. Principal Engineer
  - Based on scrutiny of circuits and layout, proprietary details
  - Hypothesis is easily tested with the loopbacks
- Test setup: loopback wires on XRTC breakout board
  - Design: 25 HR pins as outputs to other 25 as inputs
    - Testing all HR's to try to identify one with  $\mu$ SEL
  - Reverse Design: outputs and inputs swapped
  - I/O standard: 3.3V LVCMOS uses “full” level shifter
  - TCL script toggles outputs one-by-one, reporting any errors
- Results: Hypothesis #1 WRONG
  - DUTs in  $\mu$ SEL, all three: PASS
  - Controls, four unirradiated + two formerly latched: PASS
  - Control, unirradiated FT006: FAIL on one pin (AV30)



# HR I/O Functionality Testing – Digging into the Haystack



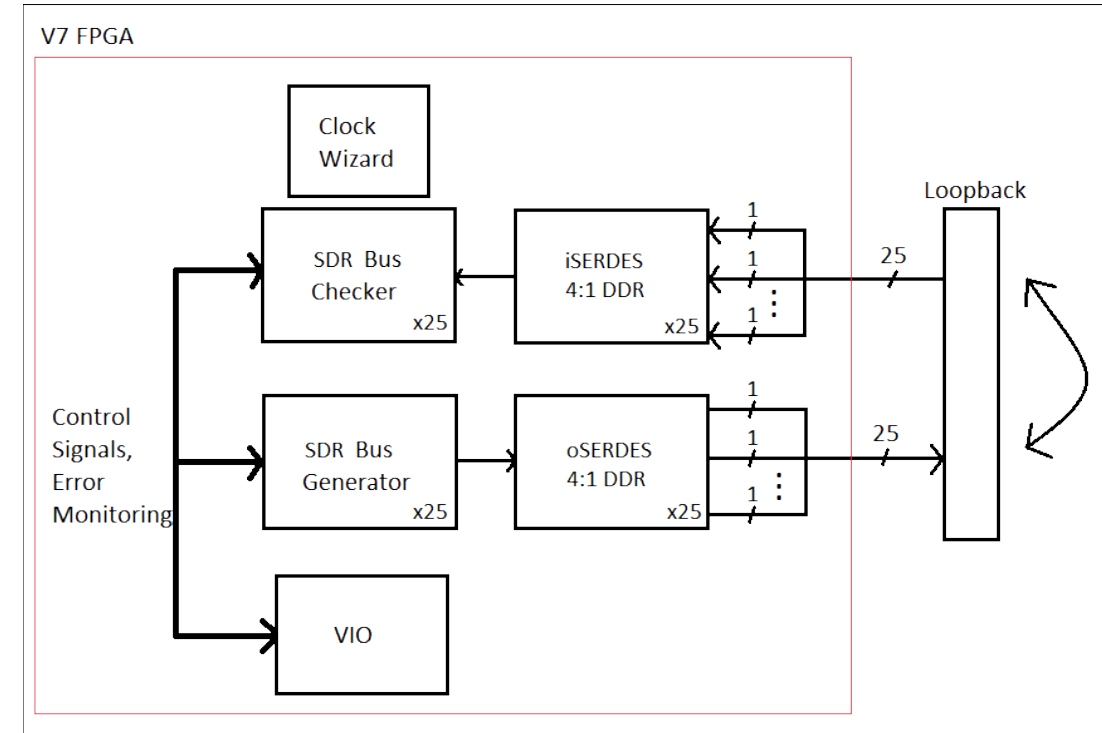
- Hypothesis #1A: Level shifter performance degradation from  $\mu$ SEL
- REFINEMENT
- Maximum operating frequency would be impacted by  $\mu$ SEL
- Test setup: slight mod of loopback setup (previous slide)
  - 24 bit loopback 'bus' as 2 pins are dedicated for clock & control
  - Again 3.3V LVCMOS I/Os, Forward and Reverse Designs
  - Generator/Checker IP patterns: 1) pseudorandom & 2) counter
  - Clock rates: 5, 10, 25, and 40 MHz (x2 using both clock edges)
- Results: Hypothesis #1A is probably WRONG
  - The three latched-up DUTs and three controls
    - Pseudorandom: PASS at 10 MHz and FAIL at 25 MHz
    - Counter Pattern: Pass at 25 MHz, FAIL at 40 MHz
  - Except one control FAIL at 25 MHz with the counter pattern
  - Fails are probably more about test fixture limitations than the FPGAs



# Another Chunk of the Haystack



- Hypothesis #2: IOSERDES fail or degradation from  $\mu$ SEL
- REFINEMENT
- Maximum operating frequency would be impacted by  $\mu$ SEL
- Test setup: loopback setup (same as previous slide)
  - 24 bit loopback 'bus' as 2 pins are dedicated for clock & control
  - Again 3.3V LVCMOS I/Os, Forward and Reverse Designs
  - Generator/Checker IP patterns: 1) pseudorandom & 2) counter
  - Clock rates: 10, 20, and 40 MHz (x2 using both clock edges)
- Results: Hypothesis #2 is probably WRONG
  - The three latched-up DUTs and three controls
    - Both patterns: PASS at 20 MHz, FAIL at 40 MHz
  - Again, fails likely from test fixture limitations, not the FPGAs

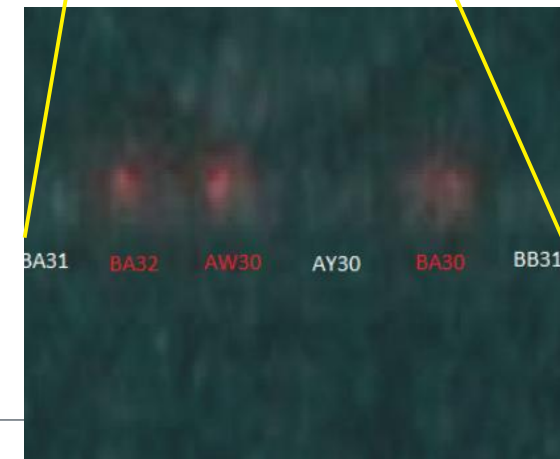




# Another Few Chunks of the Growing Haystack



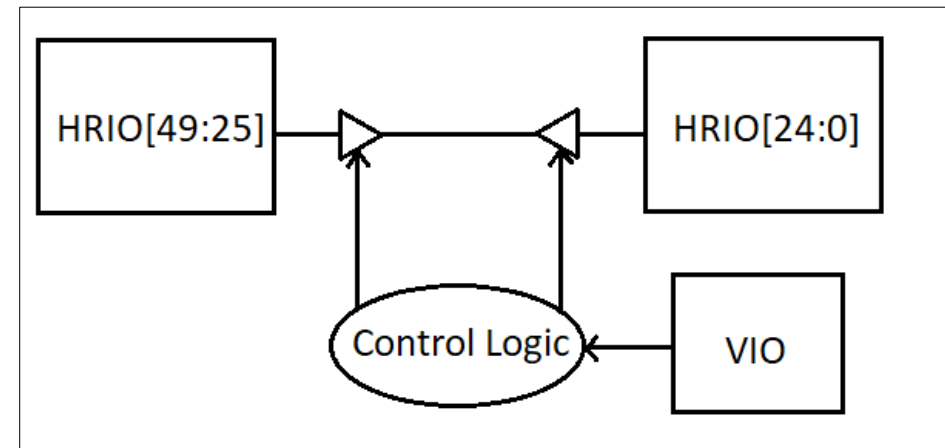
- Hypothesis #3: DC logic level degradation from  $\mu$ SEL
- Hypothesis #4: AC waveform degradation from  $\mu$ SEL
- Hypothesis #5: Level shift down degradation or fault
- Test setup: hook 'scope to outputs (instead of loopbacks)
  - Four pins checked- three suspects and one control
  - Suspects chosen mapping PEM sites for the 3 DUTs to pins → (reverse engineered map of red spots to pins may be wrong)
  - AC tests at 6 MHz
- Results: Hypothesis #3, #4, & #5 are WRONG (or pin map is wrong)
  - For all three latched-up DUTs, high and low levels measured for the selected pins are “in spec”
  - Toggling outputs looked identical on all four pins on all three latched-up DUTs (or differences are subtle)
  - Toggling 1.5V LVCMOS outputs had levels in spec and identical waveforms as well



# Deeper into the Haystack



- Hypothesis #6: Tri-State Enable or Disable Failure
- ELABORATION
- Affected pin might not tri-state when signaled
- 
- Test design:
  - Toggle BANK Tri-State Enable
  - I/O Standard: 3.3V LVCMOS
  - Direction control added so no Reverse Design needed
- Results: Hypothesis #6 is WRONG
  - No functionality problems observed



# Winnowing the Haystack, then OOPS!



- What are documented (or reverse engineered) differences between HP and HR I/Os?
  - HR's have no DCI (digitally controlled impedance) feature
    - HR "INTERM" four choices (40, 50, 60 ohm & off) ← seems like a good, next suspect
  - Some (Spartan) documentation clues that HR & HP tri-state controls are implemented differently
    - That's why we looked at bank tri-state control, but maybe there are mods to the global controls
  - Perhaps a drive strength control or circuit is involved, since these deal with higher voltages in Hrs
  - Bigger Level Shifters → Larger Area causes squeeze in layout of HP/HR common feature
    - Yikes, this grows, not winnows, the haystack: I/Os have hundreds of programmable features
  - Other ideas, anyone???
  - Needs to be a feature somehow involving (controlled by?) Vccaux
- OOPS: additional test development moot (for this presentation anyway):
- **Remaining 3 DUTs: Micro-latchups now gone**
- Not clear, what happened? Lab mishap? Power outage from hurricane + battery age?



# Future Work



- **DONE??**

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- Almost: NO plans to:

- Do lifetime testing or look for any other long-term effects

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- Almost: We DO plan to:

- Look at three more areas of possible impact: 1) drive strength, 2) termination impedance choices, or 3) global tri-state
  - Show measurements can discriminate in lab on programmed, but unlatched I/O
  - Piggyback on next available L3Harris or XRTC heavy ion beam test & induce at least one micro-Latchup
  - Perform discrimination measurements on site
  - If a functionality problem is found, cycle power and see if the problem goes away as expected

- **Hoping for a ‘non-null’ result to present in person next year; see you then...**